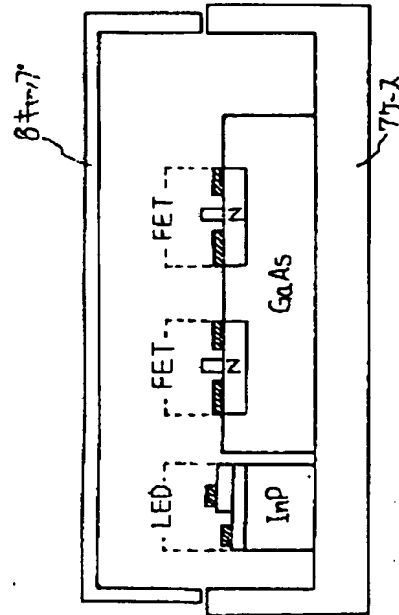


# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

PUBLICATION NUMBER : 04139877  
PUBLICATION DATE : 13-05-92  
  
APPLICATION DATE : 01-10-90  
APPLICATION NUMBER : 02264313  
  
APPLICANT : NEC CORP;  
  
INVENTOR : GOTO NORIO;  
  
INT.CL. : H01L 27/095 H01L 27/15 H01L 33/00  
  
TITLE : GALLIUM ARSENIDE FET  
INTEGRATED CIRCUIT



**ABSTRACT :** **PURPOSE:** To suppress a side gate effect which occurs when a field effect transistor(FET) is formed on the surface of a semi-insulating substrate by incorporating a light emitting element which emits light having energy within a specific range in the same package.

**CONSTITUTION:** A light emitting element which emits light having energy within a range of 1.0-1.4eV is incorporated in the same package. In other words, a GaAs integrated circuit using an N-type MESFET and InP light emitting diode(LED) having 1.24-eV energy used as a light emitting element are combined with each other so that the negative charges produced due to the negative potential of the FET can be offset by the positive charges produced by the light emitted from the adjacent light emitting element having a specific wavelength and combined with the FET. Therefore, the side gate effect can be suppressed.

**COPYRIGHT:** (C)1992,JPO&Japio